

REMARKS

Claims 1-10 remain pending in this application. Claims 1 and 5 are independent. In light of the amendments and remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. §§ 102(a) and (b) as being anticipated by *Yamasaki et al.* (USP 5,539,916); and rejected claim 5 under 35 U.S.C. §§ 102(a) and (b) as being anticipated by *Tsuboi et al.* (USP 5,140,582). Applicants respectfully traverse these rejections.

Applicants wish to thank the Examiner for indicating claims 3-4 and 6-8 contain allowable subject matter.

Claim Rejections - 35 U.S.C. § 102 - *Yamasaki et al.*

By this Amendment, Applicants have amended claim 1 to more appropriately recite the present invention. It is respectfully submitted that this amendment is being made without conceding the propriety of the Examiner's rejection, but merely to timely advance prosecution of the present application.

The present invention as set forth in claim 1, as amended, recites, *inter alia*, a self-synchronous transfer control circuit comprising a transfer control circuit, a transfer control circuit in a preceding stage, and a transfer control circuit in the subsequent stage, wherein the transfer control circuit, the

transfer control circuit in the preceding stage, and the transfer control circuit in the subsequent stage are substantially, similarly configured. It is respectfully submitted that *Yamasaki et al.* fails to teach or suggest this claim element.

The Examiner asserts in the outstanding rejection that he is relying upon element 17 of *Yamasaki et al.* to teach the transfer control circuit, I/O 12 to teach the transfer control circuit of the preceding stage and the "output of circuit 17" to teach the transfer control circuit of the subsequent stage. However, it can clearly be seen in Fig. 1 of *Yamasaki et al.* that each of these transfer control circuits are not substantially, similarly configured. As *Yamasaki et al.* fails to teach or suggest all of the claim elements, it is respectfully submitted that claim 1, as amended, is not anticipated by *Yamasaki et al.* As such, it is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claim 2 is allowable for the reasons set forth above with regard to claim 1 at least based upon its dependency on claim 1.

Claim Rejections - 35 U.S.C. § 102 - *Tsuboi et al.*

In response to Applicants' arguments filed in the Reply After Final, the Examiner responds by asserting that *Tsuboi et al.* counts the number of packets, citing to col. 23, lines 40-47. However, Applicants maintain that this teaching is insufficient in order to anticipate the present invention as set forth in claim 5.

Claim 5 clearly recites a self-synchronous transfer control circuit comprising a data transmission path holding a data packet based on a pulse signal applied from the self-synchronous transfer control circuit. In contrast, *Tsuboi et al.* discloses a packet switching system having a bus matrix switch. As depicted in Fig. 7, a clock circuit 34 is synchronized to a synchronizing signal which is also supplied to the send packet transfer controllers 211, the transfer buffers 204 and the packet switching controllers 500. As such, *Tsuboi et al.* clearly discloses a synchronous system. As the *Tsuboi et al.* system is synchronous, *Tsuboi et al.* fails to disclose a data transmission path holding a data packet based on a pulse signal applied from a self-synchronous transfer control circuit as recited in claim 5.

In addition to the above arguments, although *Tsuboi et al.* teaches counting the number of packets as asserted by the Examiner, it is respectfully submitted that this teaching is insufficient to teach the claimed invention. As recited in claim 5, the data number detection means detects the number of data based on output packet information set to the data packet. As recited in col. 23, lines 40-47, the counter 38 of *Tsuboi et al.* divides the packet information for every predetermined length (corresponding to the aforementioned time length). The divided packets are successively written into the received packet buffer 31. During this operation, the packet division number counter 38 counts the number of divided

packet frames. However, there is no disclosure in *Tsuboi et al.* that is directed to detecting the number of data based on output packet information set to the data packet. As *Tsuboi et al.* fails to teach or suggest all of the claim elements, it is respectfully submitted that claim 5 is not anticipated by *Tsuboi et al.* As such, it is respectfully requested that the outstanding rejection be withdrawn.

Additional Comments

In the Advisory Action, the Examiner asserted that nowhere do Applicants recite in the claims "where the pulse is not a clock." However, Applicants respectfully direct the Examiner's attention to new claims 9 and 10 that were added to the claim set in the Reply After Final filed December 6, 2004. It appears from the Examiner's Advisory Action that these claims were not considered. As such, it is respectfully requested that the Examiner formally consider newly-added claims 9 and 10.


Conclusion


Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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